



# **Deep-Submicrometer SOI CMOS for High Performance Integrated Circuits**

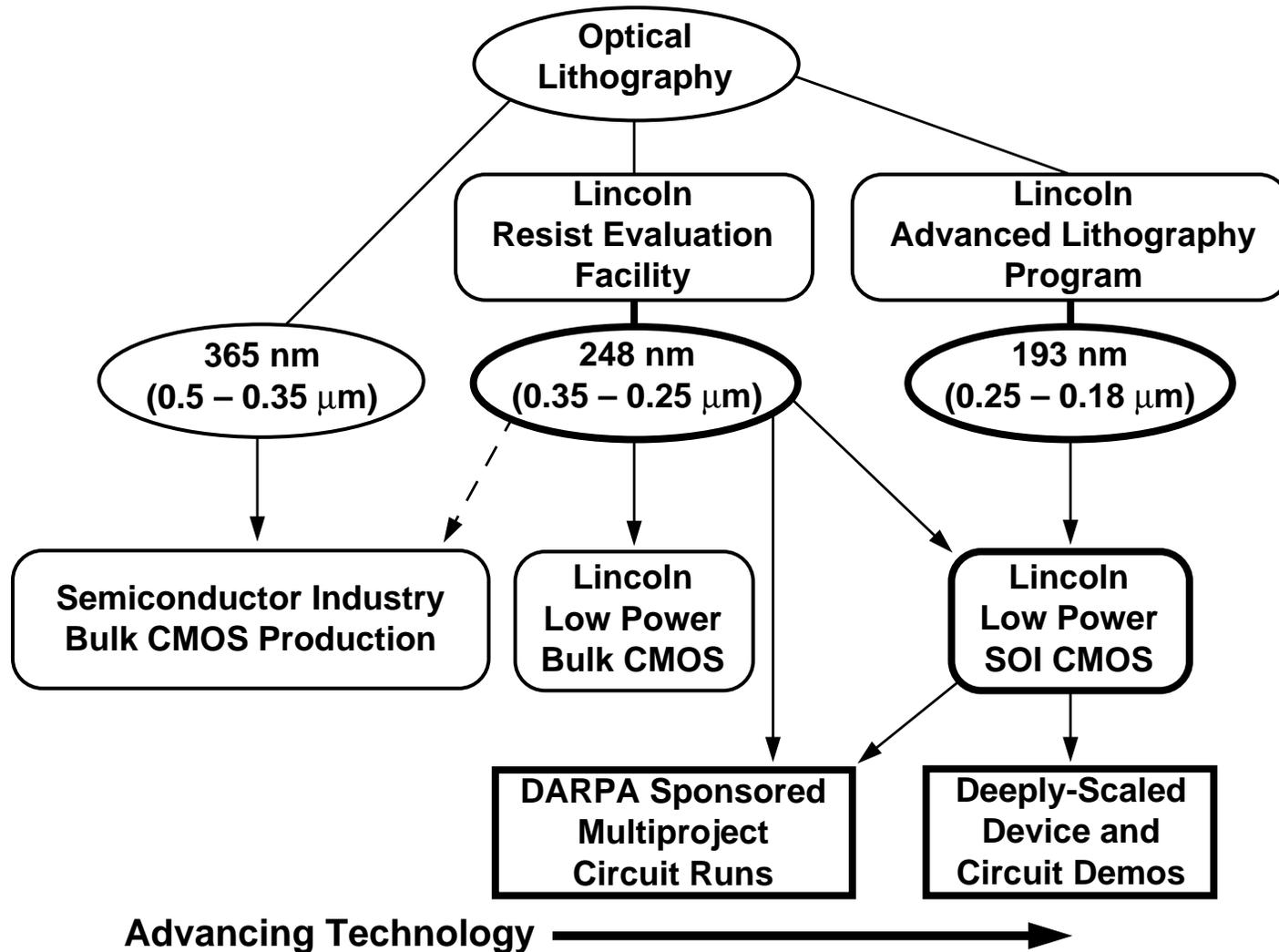
**C.L. Keast**

**MIT Lincoln Laboratory Advisory Board Meeting**

**17 April 1997**



# Outline



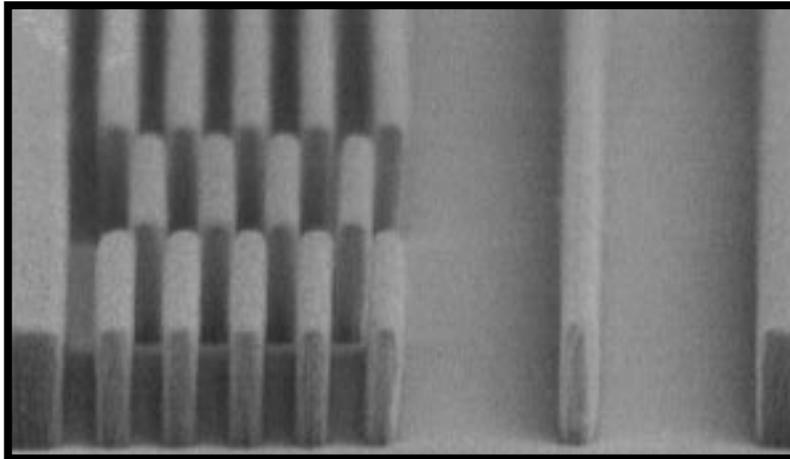


# Optical Lithography: Resolution Limits

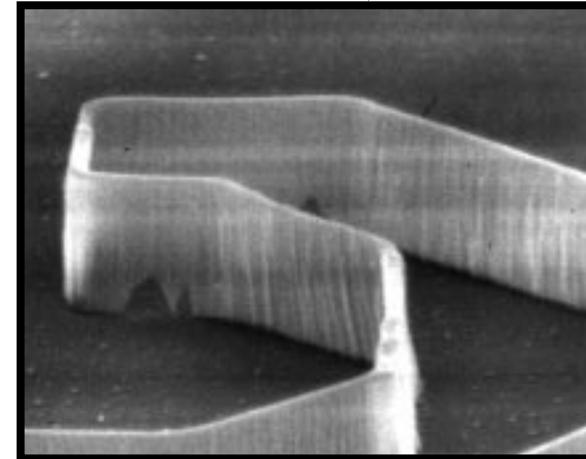
$$L_{\min} = \frac{k\lambda}{NA}$$

$k \geq 0.25$  (Diffraction Limit  $k = 0.25$ )

$\lambda$ (nm)	Feature Size ( $\mu\text{m}$ ) (NA = 0.5)		
	Conventional $k = 0.68$	Resolution Enhancements	Physical Limit
365 (Hg I-Line)	0.50	0.35	0.18
248 (DUV)	0.34	0.24	0.12
193	0.26	0.18	0.097



0.20  $\mu\text{m}$  Features Made with  
Binary Chrome on Quartz Mask



0.1- $\mu\text{m}$  Features Made with  
Phase-Shift Mask

Silylation Resist Imaged at 193 nm with 0.5 NA Step-and-Scan



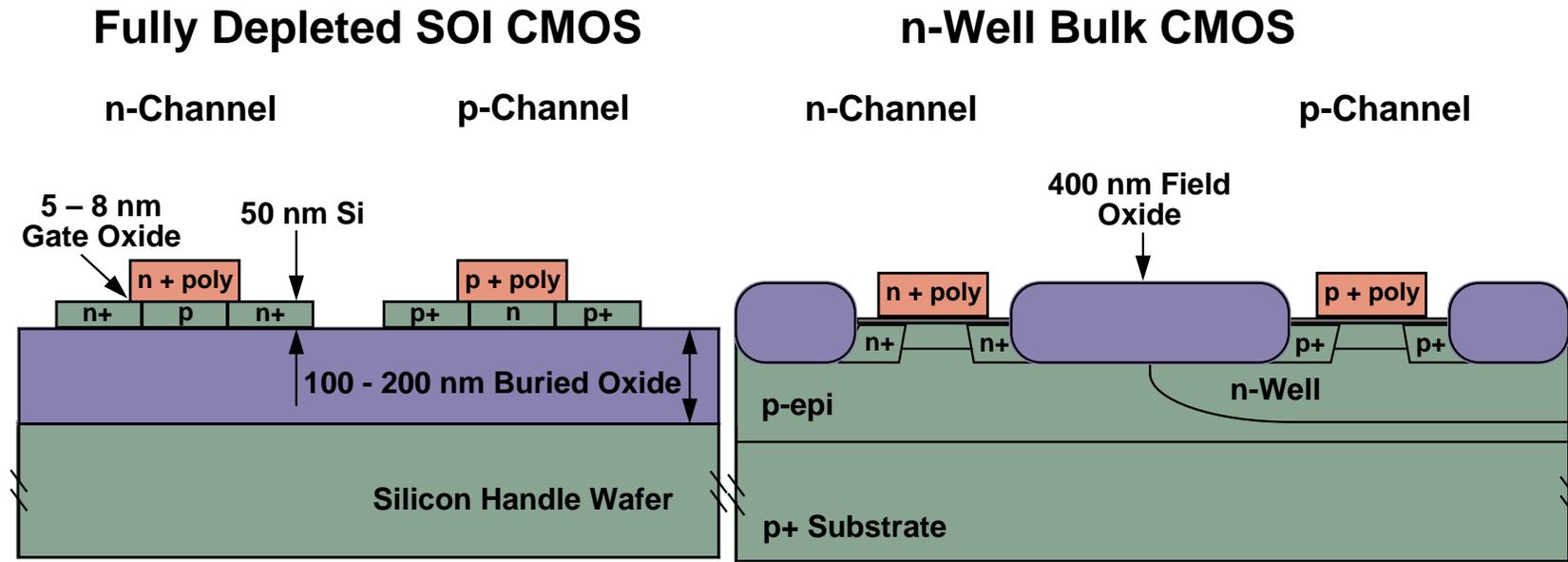
# Major CMOS Development Efforts

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- **Silicon On Insulator (SOI)**
  - Emphasis on ultra-scaled devices and very low power circuits  
900 mV power supply, 400 mV thresholds
  - 193- and 248-nm lithography
  - Currently 0.20 – 0.25  $\mu\text{m}$  gate lengths
- **Bulk silicon**
  - Emphasis on low power with analog capability  
2 V power supply, 500 mV thresholds
  - Will allow integration of advanced CMOS with CCD processors and high performance imagers
  - 248-nm lithography
  - Currently 0.25 – 0.40  $\mu\text{m}$  gate lengths



# Silicon-On-Insulator and Bulk CMOS Cross Sections



## Process Comparison

SOI has 50 nm active silicon thickness with complete oxide isolation. Each transistor is on its own silicon island. Bulk CMOS is diode isolated.

SOI allows transistors to be spaced near the minimum lithography dimension. Bulk CMOS requires well and field oxide spacing.

SOI has reduced source and drain parasitic capacitance.

Fully-depleted SOI design has near ideal subthreshold slope.



# Deep-Submicrometer SOI

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- **Program start 4/95, funded through DARPA**
  - **Process development at both Lincoln (fully-depleted SOI) and IBM (partially-depleted SOI)**
- **Lincoln program goals**
  - **Demonstration of 0.18- $\mu\text{m}$  SOI CMOS process based on 193-nm wavelength optical lithography**
  - **Make deep submicrometer experimental process available to DARPA low power research community**
    - Initial multiproject work on 248-nm lithography tool
  - **Perform collaborative work with the SOI material suppliers**



# Power and Performance of SOI CMOS

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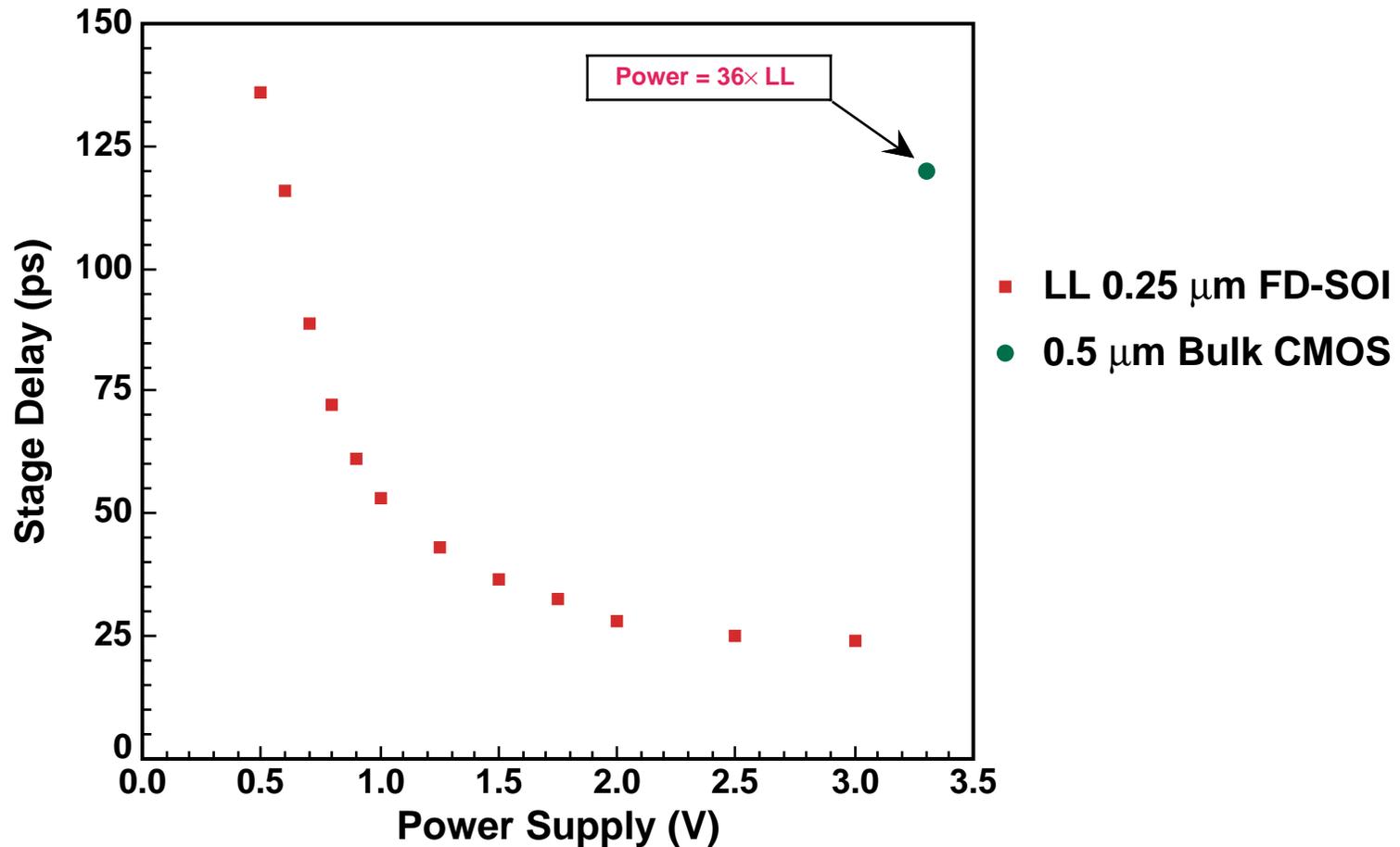
$$\text{Digital CMOS Power: } P = CV^2f$$

- **Key to lower power operation — lower V**
  - In order to maintain transistor current drive, lower power supply voltage requires lower threshold voltages
  - Improved subthreshold slope of SOI transistors allows lower threshold voltages
- **SOI also offers lower capacitance (C)**
  - Increased device packing density reduces interconnect wiring C
  - Transistor source and drain parasitic C also reduced



# Ring Oscillator Stage Delay

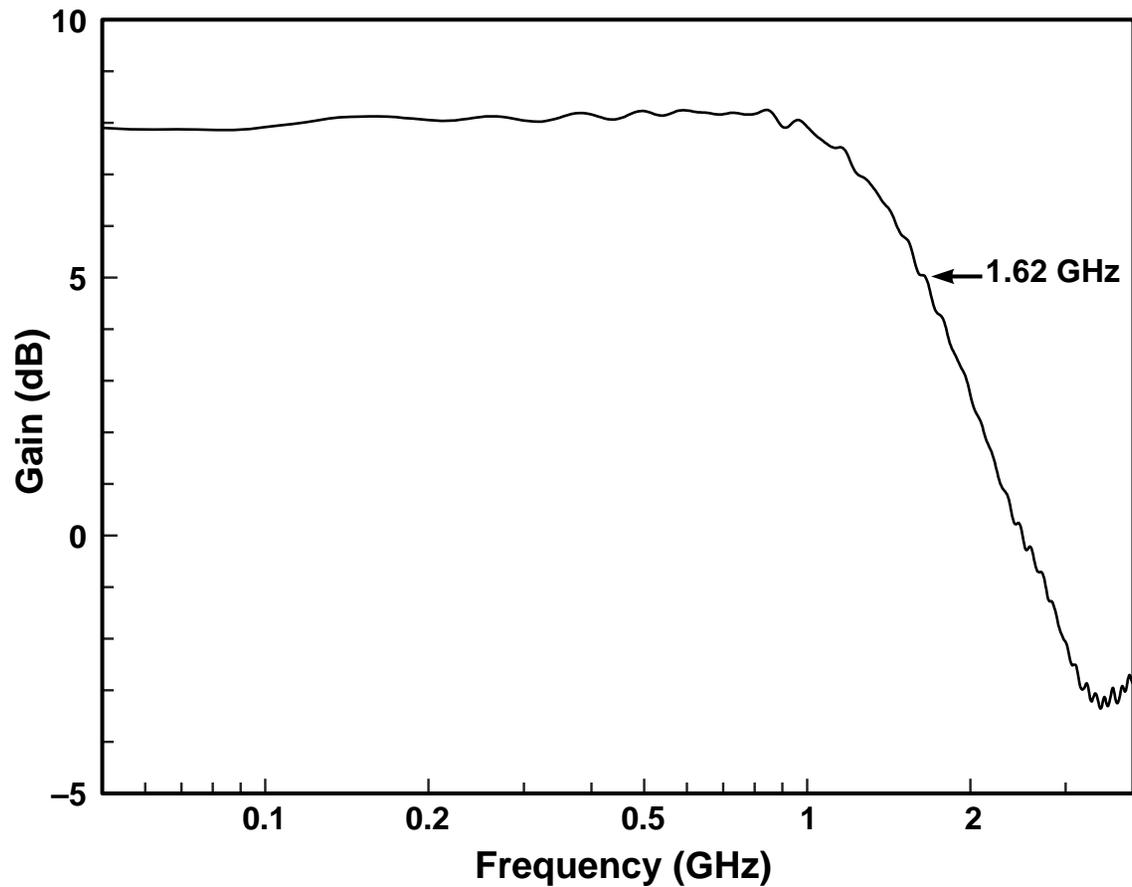
(Fanout = 1)





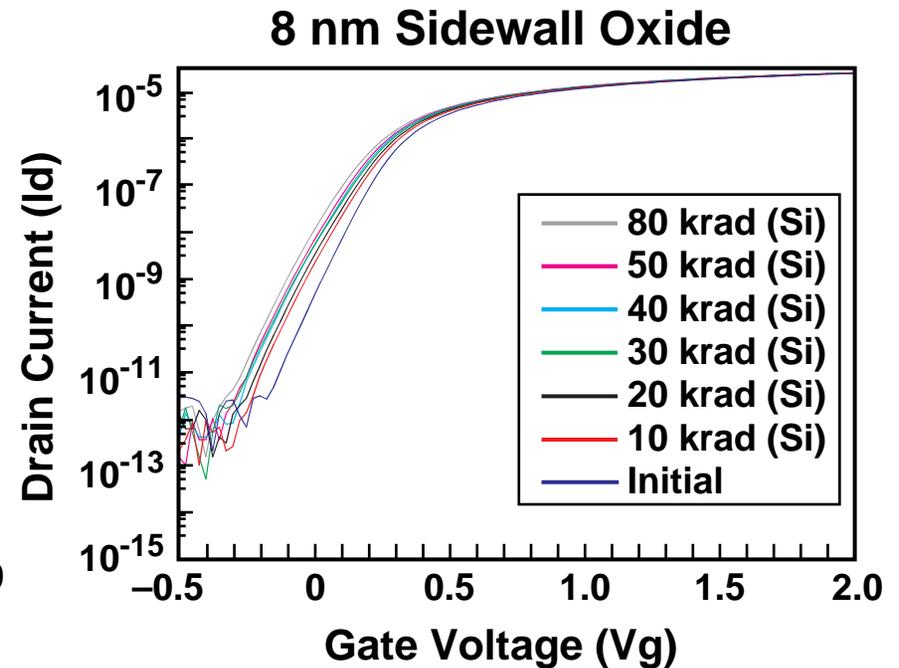
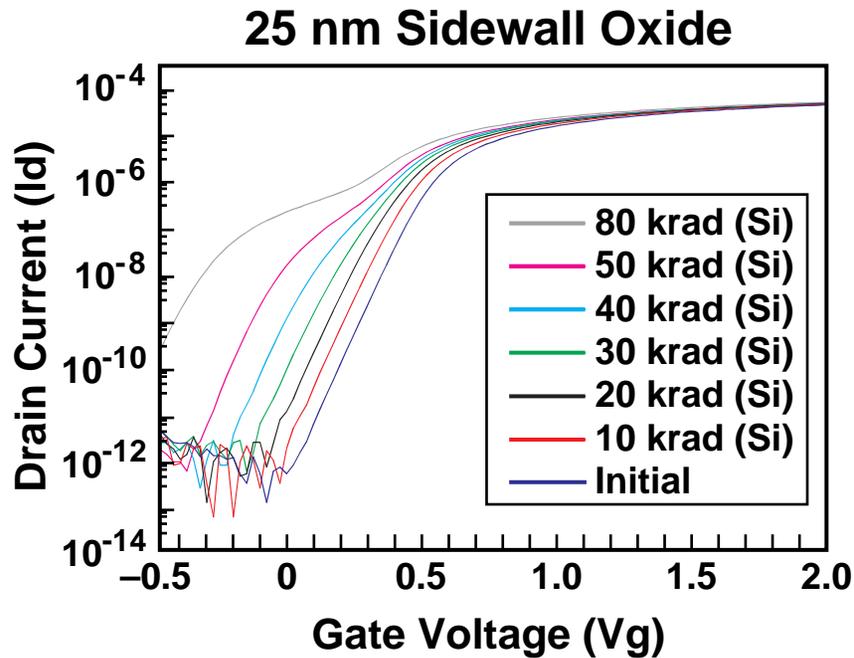
# RF Amplifier Performance

- Initial design from UC Berkeley, modified for 0.25  $\mu\text{m}$  FDSOI by Lincoln Laboratory
- Optimized redesign by Lincoln Laboratory should yield 12 dB gain, 6 GHz, 3 dB roll-off





# Low Power SOI Radiation Performance (Total Dose, X-Ray Source)





# 193-nm SOI CMOS Level Definition

**Process description: fully-depleted Silicon-On-Insulator (SOI) CMOS process with single-level poly, single-level metal, and no body contacts**

<u>Level</u>	<u>Reticle</u>	<u>Description</u>	<u>Field</u>
1	Active Area	Defines n and p Transistor Islands	Clear
2	p-Channel Mask	Implant n-Channel Island Sidewalls	Clear
3	n-Channel Mask	Implant p-Channel Island Sidewalls	Clear
4	p-Channel Mask	n-Channel Threshold Adjust Implant	Clear
5	n-Channel Mask	p-Channel Threshold Adjust Implant	Clear
6	Polysilicon Gate	Define Polysilicon Gates and Interconnect	Clear
7	n+ Implant	Implant n+ Source and Drains	Dark
8	p+ Implant	Implant p-Channel Drift Regions (Sidewall Spacer Formation)	Dark
9	p+ Implant	Implant p+ Source and Drains	Dark
10	Contact Cuts	Define Source, Drain, and Gate Contacts	Dark
11	Metal 1	Defines First-Level Metal Interconnect	Clear

**Total Photolithography Levels: 11**

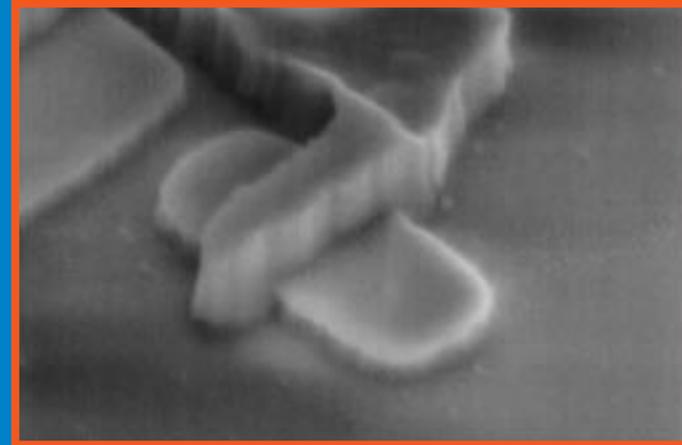
**Total Reticle Count: 8**



# All 193-nm Lithography SOI CMOS

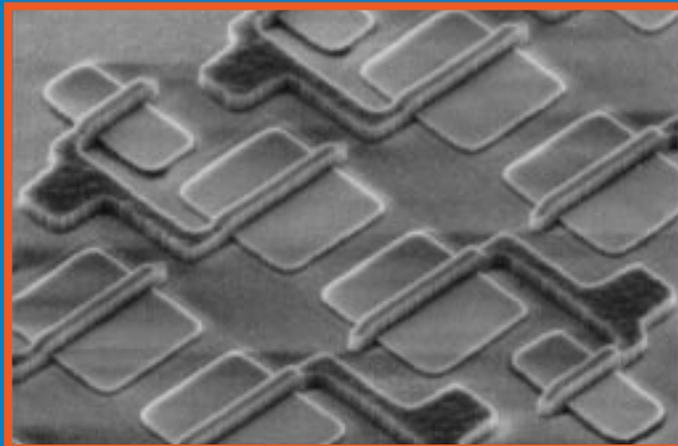
## 0.2 $\mu\text{m}$ Ring Oscillator (Gate Definition)

- World's first all 193-nm lithography CMOS run
- Low power, fully-depleted SOI device design
- 50 nm active silicon, Mesa isolated
- 250 nm dual-doped polysilicon gates



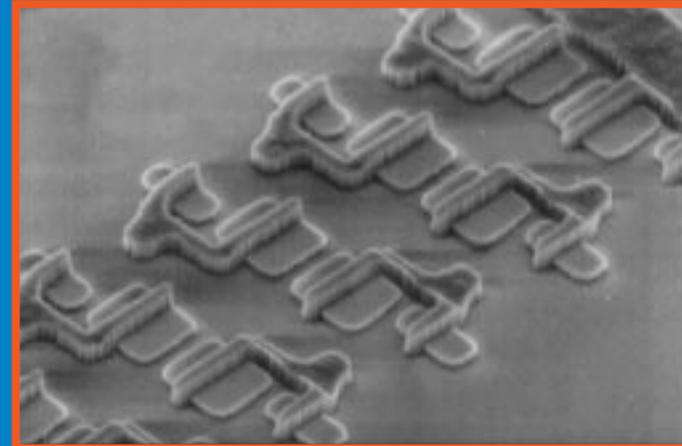
100 nm

0.2  $\mu\text{m}$  Gate Length, 0.35  $\mu\text{m}$  Rules

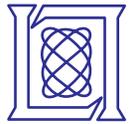


1  $\mu\text{m}$

0.2  $\mu\text{m}$  Gate Length, 0.2  $\mu\text{m}$  Rules



1  $\mu\text{m}$



# First 193-nm Lithography SOI CMOS Lot

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- **General objective**
  - Demonstration of the feasibility of using 193-nm lithography for CMOS circuit fabrication
- **Lot started 11/20/95, completed fabrication 3/6/96**
  - All levels were done with 193-nm lithography
  - Same process flow as 248-nm lots, "standard" SIMOX material
- **Utilizes process development reticle set — similar to 248-nm set**
  - 22 mm × 32.5 mm die size, six fields on 100 mm wafer
  - 0.2 μm to 1.0 μm ring oscillators, 0.1 μm to 50 μm transistors, 0.25 μm RF amplifier



# First SOI CMOS Multiproject Run

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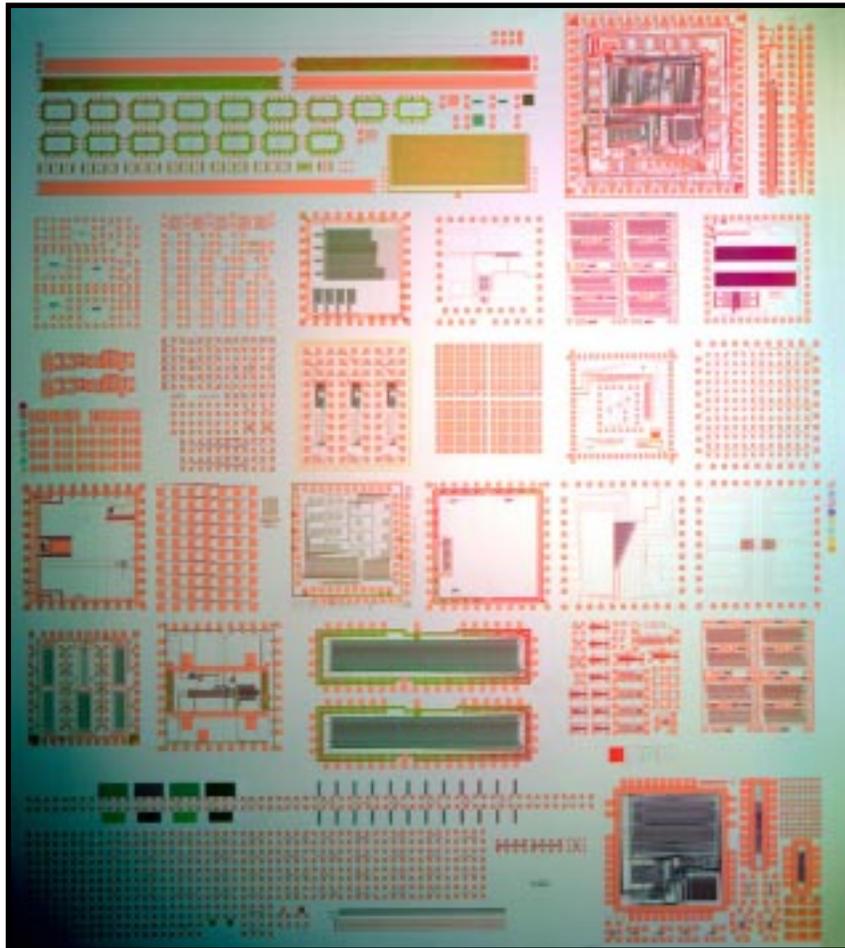
## 0.25 $\mu\text{m}$ Process, 248-nm Lithography

- **29 different designs from industry, government labs, and universities**
- **Industry**
  - Boeing, DEC, Honeywell, Irvine Sensors, Lucent, Rockwell
- **Government laboratories**
  - Lincoln Laboratory, NASA JPL, NIST, and Phillips Laboratory
- **Universities/Nonprofits**
  - ASU, Georgia Tech, Mayo, MIT, UC Berkeley, Stanford
- **Status: fabrication started 5/96, complete 9/96**

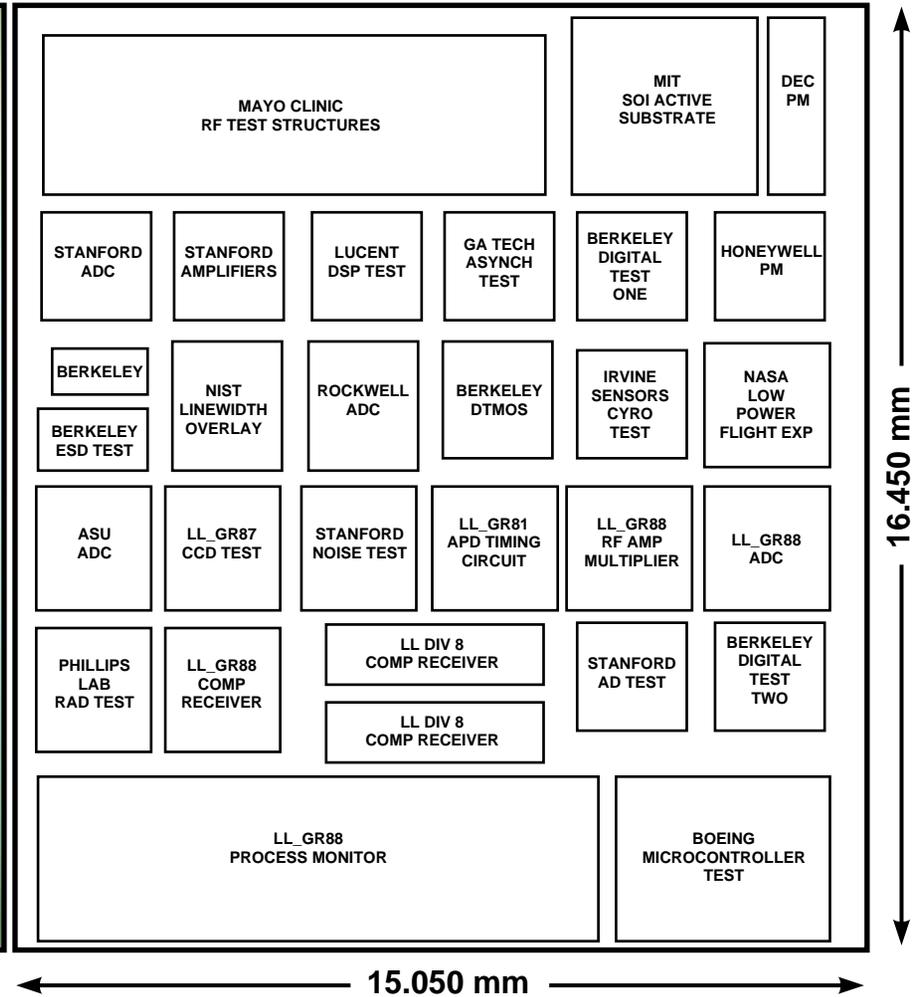


# Multiproject One (0.25 $\mu\text{m}$ FDSOI CMOS)

Die Photo

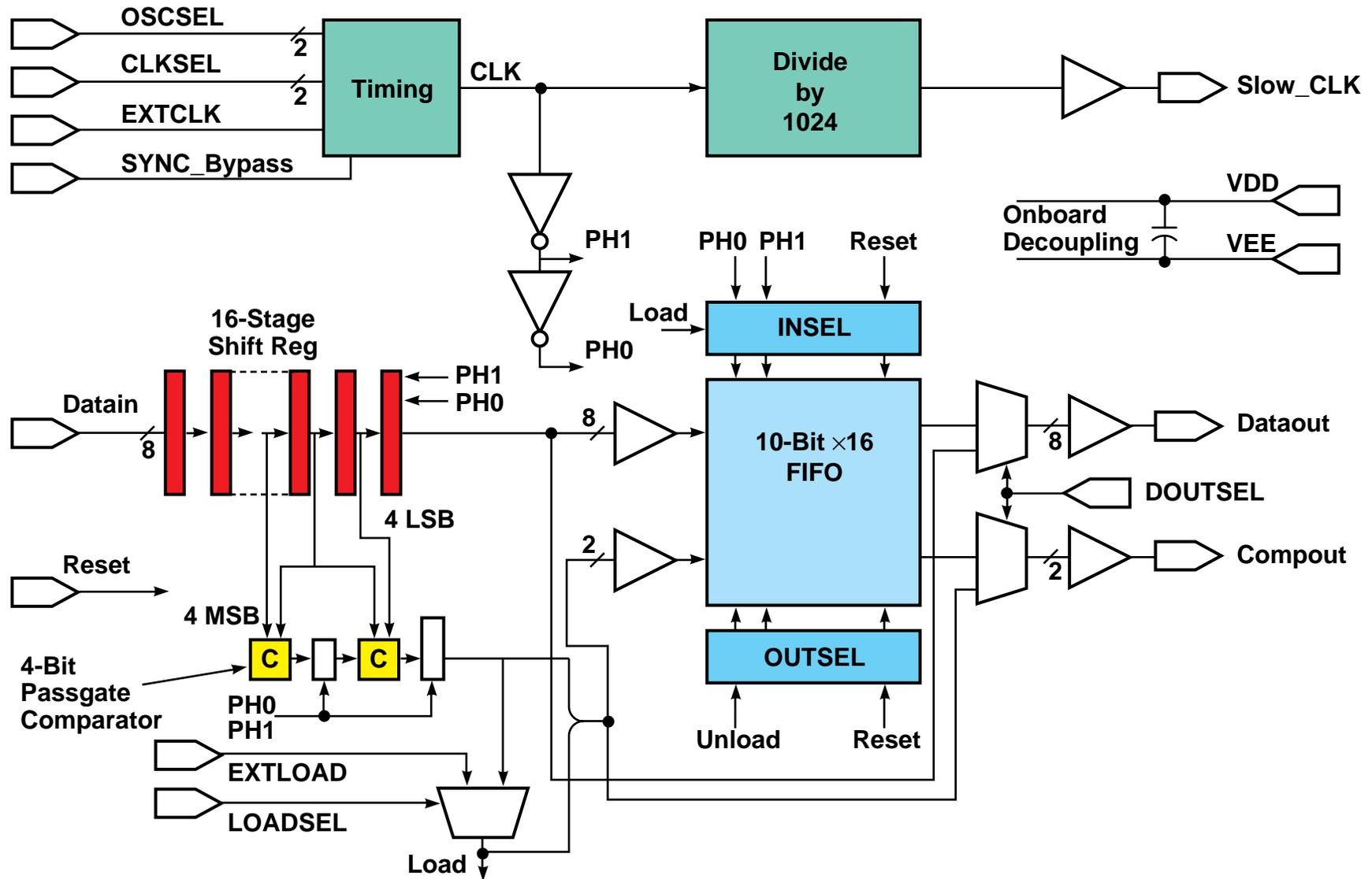


Die Map





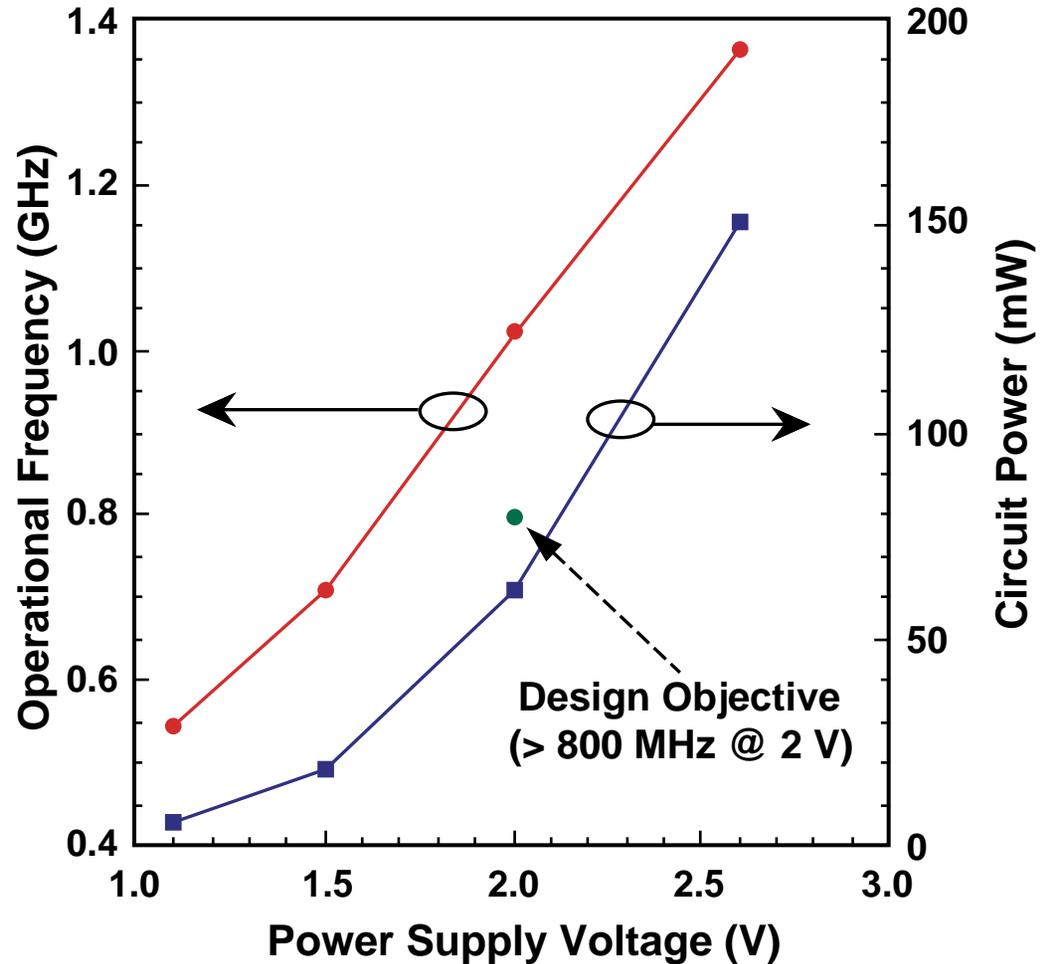
# Low Power SOI Test Chip for Compressive Receiver





# Compressive Receiver Test Circuit Results

(0.25  $\mu\text{m}$  SOI CMOS)





# Plans For The Future

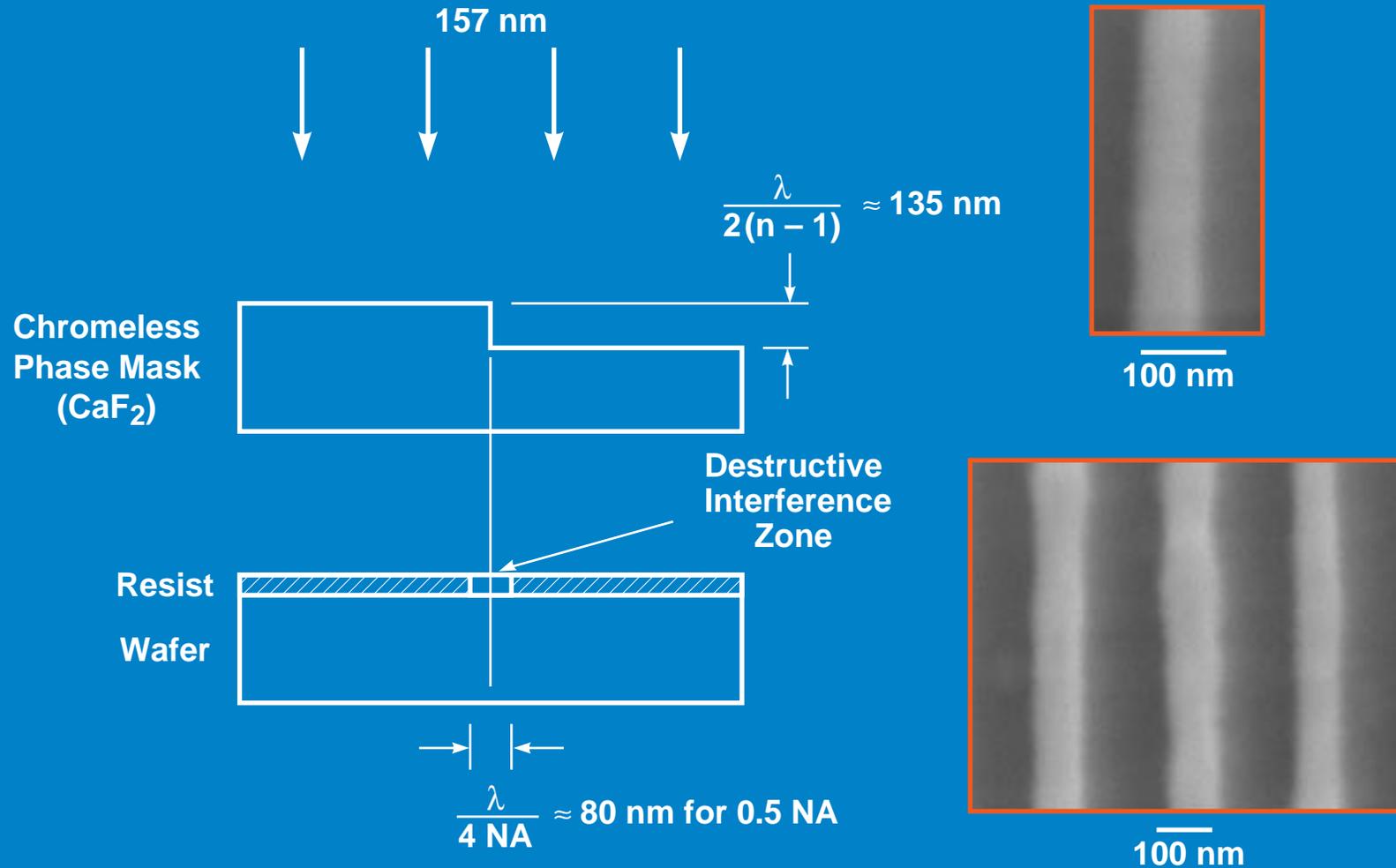
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- **Extending Optical Lithography**
  - **157 nm, 126 nm Wavelengths**  
Requires Research in: Optical Materials, Lens Design, and Resists
  - **Resolution Enhancements at 193 nm Wavelength**  
Phase Shift Reticles, Off-Axis Illumination
- **Advanced CMOS - Continue Leveraging Lithography Work**
  - **0.1  $\mu\text{m}$  Gate Length Circuit Fab using 193-nm Phase Shift Lithography (Summer 97)**  
25 nm Device Research Underway
  - **Second Multiproject Run Underway, Third Planned for Fall 97**
  - **Process Module for MCM-D/CMOS (RF Applications)**



# 157 nm Projection Microlithography

## Chromeless Phase Shift Mask





# Summary

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- **Developed Sub-0.25  $\mu\text{m}$  Fully Depleted SOI (FDSOI CMOS Process For Low Power, High Performance Applications**
  - **50-nm-Thick Active Area, Thin Silicide Formation, Fully Planar 3-Level Metal Interconnect**
- **Demonstrated World's First All 193-nm Lithography CMOS Run Using Fully Scaled 0.2 $\mu\text{m}$  Design Rules**
  - **Ring Oscillator Stage Delays of 53 ps @ 1v and 28 ps @ 2V**
- **Complex 0.18  $\mu\text{m}$  Circuit Fab Using 193-nm Lithography Scheduled for This Summer**
  - **Run Will Include 0.1 mm Phase Shifted Gate Test Circuits**



# Summary (Continued)

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- **Completed first 0.25  $\mu\text{m}$  FDSOI CMOS multiproject run using 248-nm lithography**
  - 29 different designs from 16 different organizations
  - First pass success data thinning circuit operating at 1.0 GHz and 2V
- **Second multiproject run now entering fab**
  - 29 different designs from 18 different organizations  
Circuit complexity ~100k transistors
- **Third run scheduled for Fall 97**
  - Digital receiver ASIC? (~2500k transistors)



# Conclusion

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- **Coupling of MIT Lincoln Laboratory's work in advanced optical lithography with aggressive high performance CMOS process development allows a unique DoD circuit look ahead capability.**